CLAIMS:

1. A LC controllable oscillator (LCCO) (1) comprising

- a voltage controlled oscillator (VCO) (102), a first voltage controlled current source (VCCS) of a first type (101) for supplying a current (104) to the VCO (102), the VCO being realized with a first pair (301) of VCCS of the first type coupled with a second pair (302) of VCCS of a second type and a LC resonator adapted for generating a periodical oscillation frequency which is controllable by a control signal (V),

- a first (SUP) conductor and a second (REF) conductor for connection to an external direct voltage source (105) characterized in that

- the LCCO (1) further comprises a replica scaled bias module (RSBM) (103) supplied from the external voltage source (105) via the first conductor (SUP) and the second conductor (REF),

- the RSBM (103) is conceived to generate a control signal (BIAS CONTROL) for controlling the supplied current (104) delivered by the first VCCS (101) to the VCO (102).

2. A LCCO (1) as claimed in Claim 1 wherein the RSBM (103) comprises a second (201), a third (202) and a fourth (203) VCCS, the second and the third VCCS being of the first type, the fourth VCCS being of the second type.

3. A LCCO (1) as claimed in Claim 1 in which the RSBM (103) further comprises a current source of the first type (205) and a fifth VCCS of the second type (204) that are coupled in a first input node (I1) of a differential voltage controlled voltage source (VCVS) (206) that further comprises a second input (I2) that is coupled with the fourth VCCS (203) for supplying the signal (BIAS CONTROL) for controlling the supply current (104) in the VCO (102).

4. A module (300) comprising a LCCO (1) as claimed in Claim 1 coupled with a phase shifter (301), controlled by the control signal (V), the phase shifter (301) being conceived to provide a first intermediate signal (S1) and a second intermediate signal (S2) to

an adder (SUM) (302), for adding the intermediate signals S1 and S2 to each other for obtaining a signal (S) to be supplied to a first wide band amplifier (TIA) (304) for obtaining a first output signal (I), and to a subtraction circuit (DIF) (303) for subtracting the intermediate signals S1 and S2 from each other for obtaining a signal (D) to be supplied to a second wide band amplifier (TIA) (305) for obtaining a second output signal (Q).

5. A module (300) as claimed in Claim 5 characterized in that the signals S1 and S2 are mutually phase shifted with 90 degrees.

6. A module (300) as claimed is Claim 6 characterized in that the output signals (I) and (Q) are periodical and mutually in quadrature.

7. A communication arrangement (400) for communicating via a bi-directional communication channel (404), characterized in that it comprises a receiver (401) that comprises a data and clock recovery (DCR) circuit (402) comprising a module (300) as claimed in Claim 6, the receiver being arranged for generating an output vector of signals (OUT1) by combining a received signal (IN) received from the channel (404) with the periodical signals (I) and (Q), the arrangement further comprising an emission module (403) for emitting an emission signal (OUT) to the channel (404), the emission module being conceived to generate the emission signal by combining the periodical signals (I) and (Q) with an input signal vector (IN1) in a phase locked loop (PLL) circuit (405) that contains the module (300).